Q.P. Code: 16EC424 **R16**

Reg. No: | | | | | | | | | | |

SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY:: PUTTUR

(AUTONOMOUS)

B.Tech III Year II Semester Regular Examinations May 2019

DIGITAL IC APPLICATIONS

(Electronics and Communication Engineering)

Time: 3 hours Max. Marks: 60

(Answer all Five Units **5 x 12 = 60** Marks)

UNIT-I

1	**a**	Design a 4-input CMOS AND-OR-INVERTER gate .draw the logic diagram and Functional table.	8M
	b	Draw the CMOS inverter and explain its behavior for LOW and HIGH outputs.	4M
		OR	
2	**a**	Design a three input NAND gate using diode logic and a transistor inverter. Analyze the circuit with the help of transfer characteristics.	8M
	b	Explain the following terms with reference to TTL gate. i) D.C noise margin ii) Logic levels.	4M

UNIT-II

3	**a**	Design a logic circuit to detect prime number. Write the VHDL program for it.	4M
	b	Design the logic circuit and write a data-flow style VHDL program for the following function. F (P) = ∑A,B,C,D (1,5,6,7,9,13) + d(4,15).	8M
		OR	
4	**a**	Explain the various data types supported by VHDL. Give the necessary examples.	6M
	b	Explain about VHDL program structure.	6M

UNIT-III

5		Write a behavioral VHDL code for a74X280 (9 input parity checker)	12M
		OR	
6	**a**	With the help of logic diagram explain 74×157 multiplexer.	6M
	b	Write the data flow style VHDL program for this IC.	6M

UNIT-IV

7		Design a bit LFSR counter using 74x194.List out the sequence assuming that the initial state 1	12M
		OR	
8		Write a VHDL code for a serial adder using mealy type FSM.	12M

UNIT-V

9		Write a VHDL code for 8 bit comparator circuit. Using this entity write a VHDL code for 24 bit Comparator. Use the structural model for it.	12M
		OR	
10		What is a dual priority encoder? Explain. And write VHDL code for it.	12M

*** END ***